Amendment to the Claims

1. (Currently Amended): A computer system comprising:

at least two processing units having different energy efficiencies and adapted to at least execute tasks based upon processing requirements of the tasks and a corresponding processing capability; and

a scheduler adapted to schedule a given task for execution by one of said at least two processing units so as to consume a least amount of energy, and to reschedule the given task for execution by an other of said at least two processing units when a determination indicates that said one of said at least two processing units is unable to accommodate execution of the given task based upon the processing requirements of the given task and the corresponding processing capability;

wherein said scheduler is further adapted to send a first request interrupt for execution of the given task to one of said at least two processing units in an order based on an attribute list;

wherein said one of said at least two processing units are further adapted to return one of an accept interrupt and a reject interrupt ~~the tasks for execution~~to said scheduler in response to said first request;

wherein said scheduler is further adapted to send a second request interrupt for execution of the given task to an other of the at least two processing units in the order based on the attribute list, if said scheduler receives the reject interrupt from said one of said at least two processing units.

2. (Original): The computer system according to claim 1, wherein the processing requirements comprise an end time at which the given task is to be completed.

3. (Original): The computer system according to claim 1, wherein said scheduler is a function embodied within a hardware component other than said at least two processing units.

4. (Original): The computer system according to claim 1, wherein one of said at least two processing units comprise said scheduler.

5. (Original): The computer system according to claim 1, wherein said scheduler is further adapted to intercept interrupts from said at least two processing units and peripheral devices.

6. (Original): The computer system according to claim 1, wherein said at least two processing units share memory space.

7. (Original): The computer system according to claim 1, wherein said at least two processing units share input/output space.

8. (Original): The computer system according to claim 1, wherein said at least two processing units share input/output space, and said scheduler and said at least two processing units share memory space.

9. (Original): The computer system according to claim 1, further comprising a task attribute store adapted to store at least some of the processing requirements of at least some of the scheduled tasks.

10. (Original): The computer system according to claim 1, wherein the determination is made by said scheduler.

11. (Original): The computer system according to claim 1, wherein the determination is made by said one of said at least processing units.

12. (Cancelled).

13. (Original): The computer system according to claim 1, wherein the processing requirements comprise a processing capacity required to execute the given task.

14. (Currently Amended): A computer system comprising:

a plurality of processing units, each of the plurality of processing units adapted to execute tasks thereon, and at least two of the plurality of processing units having different energy efficiencies; and

a scheduler adapted to schedule a given task for execution by one of said plurality of processing units by querying said plurality of processing units in a partial order of descending energy efficiency to one of accept and reject the execution of the given task until one of the given task is one of accepted and executed by said one of said plurality of processing units and the given task is rejected by all of said plurality of processing units;

wherein said scheduler is adapted to schedule the given task in an order based on an attribute list, wherein the attribute list comprising a plurality of attributes, said plurality of attributes comprising (a) a task identification number of the given task, (b) a quantity of said plurality of processing units capable of executing the given task, (c) a processor identification number for each of the quantity of said plurality of processing units capable of executing the given task, (d) an address of the location of the given task associated with each of the of the quantity of said plurality of processing units capable of executing the given task; and (e) a worst case quantity of processing unit cycles for timely executing the given task for each of the quantity of said plurality of processing units capable of executing the given task.

15. (Original): The computer system according to claim 14, wherein said scheduler is a function embodied within one of said plurality of processing units.

16. (Original): The computer system according to claim 14, wherein said scheduler is a function embodied within a hardware component other than one of said plurality of processing units.

17. (Original): The computer system according to claim 14, wherein said scheduler intercepts interrupts from each of said plurality of processing units and peripheral devices.

18. (Original): The computer system according to claim 14, wherein said plurality of processing units share memory space.

19. (Original): The computer system according to claim 14, wherein said plurality of processing units share input/output space.

20. (Original): The computer system according to claim 14, wherein said plurality of processing units share input/output space, and said scheduler and said plurality of processing units share memory space.

21. (Original): The computer system according to claim 14, further comprising a task attribute store adapted to store at least some of the processing requirements of at least some of the tasks.

22. (Original): The computer system according to claim 14, wherein said scheduler is further adapted to exclude any of said plurality of processing units from the partial order based upon at least one predefined condition.

23. (Original): The computer system according to claim 14, wherein the processing requirements comprise a processing capacity required to execute the given task.

24. (Currently Amended): A computer system comprising:

at least two processing units having different energy efficiencies and adapted to one of accept and reject scheduled tasks based upon processing requirements of the scheduled tasks and a corresponding processing capability, and to at least execute the scheduled tasks that are accepted; and

a scheduler adapted to schedule a given task for execution by one of said at least two processing units so as to consume a least amount of energy, and to rescheduled the given task for execution by an other of said at least two processing units when said one of said at least two processing units rejects the execution of the given task;

wherein the scheduler is adapted to send a request interrupt to each of the at least two processing units in an attribute list, one processing unit at a time, for requesting whether the each of the at least processing units is capable of executing the given task;

wherein the scheduler is adapted to send the request interrupt to each of the at least two processing units in the attribute list until one of (a) the one processing unit sends an accept interrupt to the scheduler accepting the given task, and (b) all of the at least two processing units in the attribute list send a reject interrupt to the scheduler rejecting the given task.

25. (Original): The computer system according to claim 24, wherein said scheduler is a function embodied within a hardware component other than said at least two processing units.

26. (Original): The computer system according to claim 24, wherein one of said at least two processing units comprise said scheduler.

27. (Original): The computer system according to claim 24, wherein said scheduler is further adapted to intercept interrupts from said at least two processing units and peripheral devices.

28. (Original): The computer system according to claim 24, wherein said at least two processing units share memory space.

29. (Original): The computer system according to claim 24, wherein said at least two processing units share input/output space.

30. (Original): The computer system according to claim 24, wherein said at least two processing units share input/output space, and said scheduler and said at least two processing units share memory space.

31. (Currently Amended): A computer system comprising:

a plurality of processing units, each of the plurality of processing units adapted to execute tasks thereon, and at least two of the plurality of processing units having different energy efficiencies;

a processor attribute table adapted to store processing capability information for at least some of said plurality of processors and to update the processing capability information dynamically when the processing capability information changes, wherein the processing capability information comprises (a) processing requirements of a given task, and (b) processing capability for at least some of the plurality of processing units for executing the given task; and

a scheduler adapted, for ~~a~~ the given task, to retrieve at least some of the processing capability information from said processor attribute table in one of a partial order and a strict order of descending energy efficiency until one of the plurality of processors is found to possess adequate processing capability with respect to task processing requirements for the given task, and to schedule the given task for execution by said one of the plurality of processors.

32. (Original): The computer system according to claim 31, wherein said computer system further comprises at least one functional block adapted to perform at least one function associated with an interrupt.

33. (Original): The computer system according to claim 31, wherein said computer system further comprises at least one functional block adapted to perform at least one function utilized by a task.